

What is claimed is:

1. A memory system comprising:
 - 5 a circuit board having a first means for receiving and a second means for receiving;
a first memory module received in said first means for receiving;
 - 10 a second memory module received in said second means for receiving; and
 - 15 a flexible bridge connecting said first and second memory modules for providing a signal bus between said memory modules.
2. The memory system of claim 1, wherein the memory modules are received in the respective means for receiving at a first side thereof and wherein the flexible bridge extends from a respective second side of the memory modules.
- 25 3. The memory system of claim 1, wherein the respective second side of the memory module is arranged opposite to the first side thereof.
4. The memory system of claim 1, wherein the receiving means are slots for receiving memory modules adapted for DDR memory systems.
- 30 5. The memory system of claim 1, wherein the flexible bridge comprises data lines and/or control signal lines for providing a data bus and/or a control signal bus between said memory modules.
- 35 6. The memory system of claim 1, wherein a memory controller and signal lines are provided on said circuit board, wherein said signal lines provide a data bus and/or a control signal bus between said controller and said first memory module.

7. The memory system of claim 6, wherein said signal lines on said circuit board further provide a clock bus between said memory controller and said memory modules.

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8. The memory system of claim 6, further comprising a third memory module received in a third means for receiving and wherein said signal lines on said circuit board further provide a data bus and/or a control signal bus between said second and said third memory modules.

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9. The memory system of claim 1, wherein the bridge is a flexible printed circuit board having a ground layer and a signal layer.

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10. The memory system of claim 1, wherein said signal bus provided by said flexible bridge has a trace impedance adapted to a trace impedance of buses on the memory module and the circuit board to which said signal bus is connected.

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11. A memory subsystem comprising:

a first memory module, a second memory module, and a flexible bridge connecting the first and the second memory modules and providing a signal path therebetween.

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